International Journal of Engineering Trends, Management & Medical Sciences
ISSN: XXXX-XXXX

FULLY-DYNAMIC NOISE AWARE THREE-STAGE LOW POWER COMPARATOR USING ERC

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ABSTRACT

This project proposal presents the three-stage comparator and its upgraded version, which aims to reduce kickback noise and boost speed. Compared to traditional two-stage comparators, the three-stage comparator employed in this study has an extra amplification step that increases speed and voltage gain. Unlike the traditional two-stage construction, which uses pMOS input pair in the regeneration stage, the three-stage comparator allows the use of nMOS input pairs in both the regeneration and amplification stages, significantly increasing the speed. Furthermore, a CMOS input pair is used in the amplification step of the proposed improved three-stage comparator. This greatly reduces the kickback noise by canceling out the nMOS kickback via the pMOS kickback. It also provides a second signal line during the regeneration step, which helps to increase speed even more quickly. For ease of comparison, the conventional two-stage comparator and the recommended three-stage comparator are both built in the same CMOS process. Measured findings show that the enhanced version of the three-stage comparator boosts speed. By presenting an edge-race comparator (ERC), a novel kind of inventive voltage comparator that is energy-efficient, this article expands on this concept. It compares the differential input voltage by generating two propagating edges in two inverter loops and measuring the distance between the two edges. A last dash between the two edges determines the winner. Because the comparator has low power and noise, it does not need much voltage headroom. By automatically modifying its noise, power consumption, and delay dependent to the input voltage, it may save a great deal of time and energy in coarse comparisons and minimize noise in delicate comparisons.

Keywords: edge-race comparator, successive approximation register, kickback, Analog-to-digital converters, and central processing units.

I. INTRODUCTION

Comparators are extensively utilized in many different applications, including analog-to-digital conversion, voltage control, and brown-out detection. In some of these uses, the circuit's overall performance is directly impacted by the performance. An excellent example is a high-resolution successive-approximation-register (SAR) analog-to-digital converter (ADC), which, for fine bit decisions requiring a large amount of energy that takes a significant portion of the total conversion energy, requires an especially low-noise comparison to distinguish voltages that are very close.

International Journal of Engineering Trends, Management & Medical Sciences
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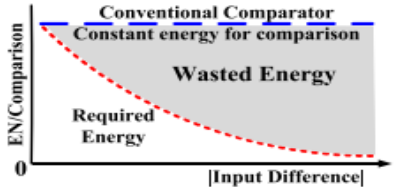
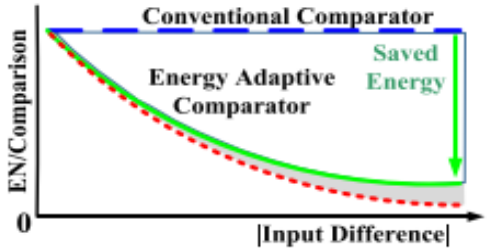


(a)

Fig. 1.Required energy for comparison versus input difference. (a) Conventional comparators wasting most energy for large input difference.



(b)

(b) Energy scaling saved wasted energy for comparison. comparator's performance as the comparator plays a key role.

But as Fig. 1(a) shows, conventional clocked comparators [1]–[3] typically consume nearly constant energy for each comparison because they are designed based on the most accurate and power-hungry comparison, even though the actual energy requirement decreases sharply as the input signal difference increases. As a result, in these sorts of applications, modifying the comparison energy based on the input difference level may significantly aid in lowering both the overall energy consumption and the total comparison energy [Fig. 1(b)]. Due to this, some earlier research on SAR ADCs presented methods for scaling comparator energy [4]–[10]. These methods included time-domain comparators whose noise level could be adjusted by varying the length of the delay lines [8], dual ADC architectures that employ two comparators for coarse and fine comparisons [4], [5], and multiple repetitive comparisons for noise-critical bits [5]–[7]. However, by adding overheads for additional control and raising the complexity of both design and operation, these structures lessen the simplicity of the SAR structure. It is also challenging to gain much from comparator energy scaling because of their limited noise tuning range and amount of energy scaling steps. Furthermore, some previous methods need preprogrammed scaling via prediction, which introduces further inefficiencies due to prediction errors. The voltage comparator is a crucial analog module that finds extensive usage in a variety of applications, including wireless sensor networks [5], memory [4], and analogto-digital converters (ADCs) [1]–[3]. Low power consumption is a crucial factor in many applications since wearable, implantable, and mobile devices are so common. The sequential approximation register (SAR) ADC architecture is the recommended design for low-power ADC implementation [6]–[9]. To get the desired speed and resolution, the SAR ADC relies on its comparator; nevertheless, the comparator consumes a significant amount of power, usually between 50 and 60 percent [10] of the entire SAR ADC power budget. To be more precise, in order to detect a tiny voltage

difference at fine LSB choices, a high-resolution SAR ADC needs a low-noise comparator, which results in substantial power consumption at LSB decisions. More importantly, as Fig. 1(a) illustrates, a traditional comparator is constructed based on the most power-hungry LSB choice, which means that it uses almost constant energy for every bit decision (across the input voltage range). However, the real energy needed at coarse MSB choices (high input voltage) is much less as the comparator noise and energy consumption do not need to be as high at coarse MSB decisions [see Fig. 1(a)]. This results in energy being wasted at coarse MSB judgments. Because of this, several methods have been put out recently to achieve energy scaling.

II. LITERATURE REVIEW

Low-power consumption CMOS switched-capacitor circuits have been used for operational amplifiers by Jan Crols et al. [1] (1994). Switched opamps: the goal is to replace the essential buttons with opamps that can be turned on and off without the need for voltage multipliers. This suggested method's primary bottleneck is its inability to scale with traffic. Analog to digital circuit technology, including a 0.6 μCMOS technology, 14.3 MS/s, and 10-bit ADC, was created by Andrew M. Abo et al. [2] (1998). A folded-cascade stage in the first stage and a common source stage in the second stage comprise a two-phase, completely differential amplifier. Regretfully, in this technique, the complexity parameter is quite high and density limitations are not lowered. The Sigma-Delta modulator, which has high performance, good baseband input, and low power, functional amplifiers, was presented by Bosco Leung et al. [3] in 1997. A second-order passive sigma-delta modulator was created in the 1.2-m CMOS phase. However, the primary shortcomings of this material are the absence of user-defined amplification and latency improvements. Using a Sigma-Delta Digital Conversion Converter, S. J. Steyaert et al. (1998) created a differential modified, dynamic, 77-dB (16 kHz) bandwidth and a 62 dB (signal-to-noise) peak ratio. Half-time integration has been used to modulator topology. Low value design methodologies and building blocks of specialized low voltage circuits, such an AB class operational transduction amplifier, a common-mode feedback amplifier, and a comparator, will be treated. Using CMOS technology, current mode signal processing has greatly improved and led to fascinating circuit design. As features get smaller and the need for high-speed, low-power applications grows, current-mode circuits are being explored as a voltage-mode circuit substitute. Because current comparators have higher precision, less noise, and need less power, they are essential parts of analog systems. It is applicable to VLSI neural networks, oscillators, A/D converters, current-to-frequency converters, sensor circuits, and portable wireless communication, among other applications. Using a simple inverter, H. Traff [1] introduced the first high speed, low input impedance current comparator. A. T. K. Tang et al. [2] and L. Ravezzi et al. [3] are two designs that have altered Tarff's method, achieving speed gains at the expense of higher power consumption. There have been many prior proposals for high-speed comparator designs. The pre-charged function block in all [6] is connected to many feedback transistors that provide additional discharge channels and shorten the comparator's latency. As we shall

demonstrate in the sequel, the design is not as quick as our high-speed design since the precharge phase is not used for any calculation.

III. EXISTING METHOD

This brief suggests a modified three-stage comparator, as seen in Fig. 4, to reduce kickback noise and increase speed even more. The improved version contains additional routes M29–32 in the latch stage of Fig. 4(c) and the extra first two stages of Fig. 4(b) compared to the original version in the preceding section. The other two levaels use a pair of pMOS inputs.

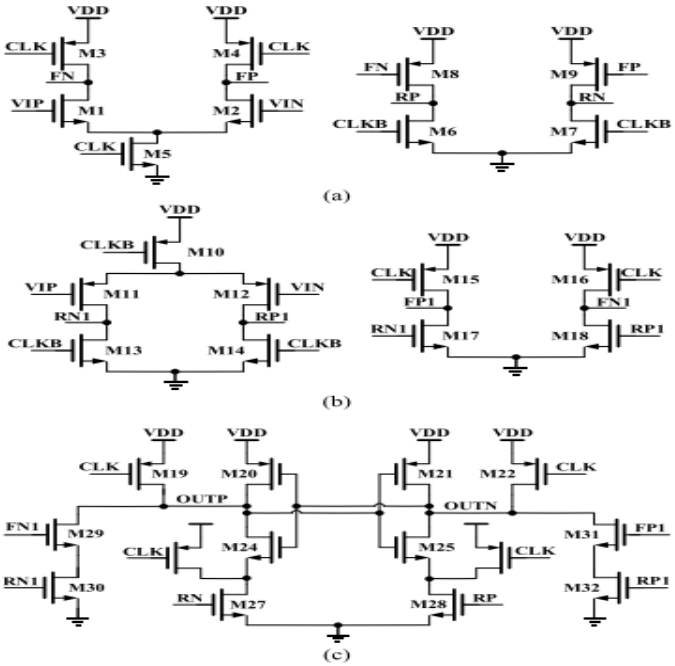


Fig. 2. Proposed modified version of three-stage comparator. (a) Original first two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

M11–12 to eliminate the kickback noise of the nMOS input pair M1-2. Additionally, the additional routes M29–32 provide additional signal to the latching nodes OUTP and OUTN, which increases regeneration speed and significantly suppresses noise and input referred offset. These additional circuits function as follows. CLK is zero and CLKB is one during the reset phase. In Fig. 2(b), FP1 and FN1 are reset to VDD, while RP1 and RN1 are reset to GND. This ensures that there is no static current in the additional route M29–32 by turning off M30 and M32 in Fig. 4(c). CLK increases to 1 and CLKB decreases to 0 during the amplification phase. In Fig. 4(b), RP1 and RN1 increase to VDD (where R denotes rise). Next, FP1 and FN1 fall to GND, where F denotes fall. The additional routes in Fig. 2(c) are switched on for a brief period of time, drawing a differential current from the latching nodes OUTP and OUTN, since the rising of RP1 and RN1 happens before the falling of FP1 and FN1. As a result, there is a differential voltage at OUTP and OUTN, which suppresses noise

and the comparator input referred offset and speeds up the regeneration phase thereafter. The other routes in Fig. 2(c) are again switched off to stop the static current when FP1 and FN1 fall to GND. Overall, the three-stage comparator that has been improved offers the following benefits: reduced input referred offset and noise, lower kickback noise, and quicker speed. High-speed, high-resolution SAR ADCs may use it. The suggested updated version, for instance, works well with the time-interleaved noise-shaping SAR ADC in [13]. Its comparator speed and comparator kickback noise restrict its ADC speed and resolution, respectively, as [13] makes clear. While channel isolation is used by Zhuang et al. [13] to lessen the impact of kickback noise, this isolation adds to the system's complexity. On the other hand, these problems may be resolved by the suggested modified three-stage comparator. When compared to other comparators, it has the quickest speed and the least amount of kickback noise.

IV. PROPOSED METHOD

EDGE-RACE COMPARATOR:

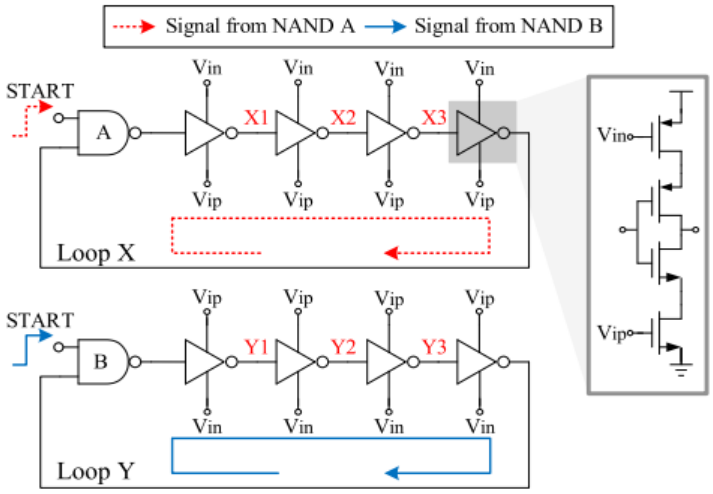


Fig.3 Proposed ERC.

Figure above depicts the suggested ERC. The above figure displays its timing diagram, which will be discussed later. The proposed ERC is made up of NAND gates and inverter delay units, much like the EPC in the preceding figure. The comparator inputs Vin and Vip additionally regulate the delay of the delay units. The distinction is that, as will be shown later, we divide the single loop into two loops in order to speed up the comparison process and lessen interference between the two edges. The suggested ERC functions as follows. The two loops are at the reset phase when START = 0. The two NAND gates produce two propagating edges in each of the two loops when START climbs to 1. As seen in Fig. 3, the two edges begin at the same beginning point and compete with one another. They spread recursively via the two loops. Due to their differing rates of propagation, the two edges' distance from one another steadily grows over time. Ultimately, the race comes to an end and the winner (comparison result) is established when the distance reaches a predetermined number, d0. The circuit shown in Fig. 3(a) may be used to assign this preset

value d0 to two inverter delays; this will be covered later. Vip> Vin occurs when the edge in loop X outperforms loop Y, and vice versa. On the other hand, as START climbs to 1, the two edges in the EPC of Fig. 2 begin at separate points in the loop.

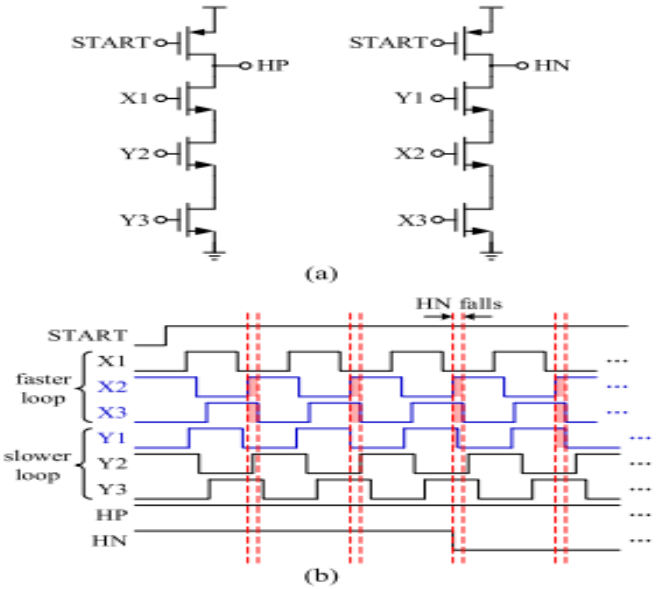


Fig. 4. (a) Circuit for measuring the distance between edges and (b) timing diagram of Vip> Vin.

As a result, five inverter delays represent the initial separation between the two edges. This gap steadily becomes smaller over time. The comparison result is produced as the distance approaches zero. Therefore, we may deduce that the preset value d0 for the EPC of Fig. 2 is 5 inverter delays. The primary benefit of the suggested ERC over the EPC is its much quicker comparison speed. This is due to the fact that the preset value d0 of the ERC (2 inverter delays) that is being suggested is 2.5 times smaller than the EPC (5 inverter delays). Furthermore, real-world applications actually employ more inverter delay units [17]; for instance, we may use 16 inverter delay units for each of Figs. 2 and 3, even though Figs. 2 and 3 only display 8 inverter delay units for clarity and ease of understanding. In this instance, 9 inverter delays are the preset value d0 of the EPC. In contrast, as we utilize an additional circuit [Fig. 4(a)] to guarantee the fixed d0, which will be discussed later, the preset value d0 of the suggested ERC is still 2 inverter delays. Therefore, in this instance, the suggested ERC's speed is 4.5 times quicker than the EPC. The circuit for determining the separation between the two propagating edges is shown in Fig. 4(a) in order to guarantee the fixed d0. The two dynamic logics that produce the comparison results HP and HN are all that are needed. The letters "P" and "N" stand for positive and negative outputs, respectively. Both HP and HN are reset to high (where "H" stands for high) during the reset phase (START = 0). In the meanwhile, the NAND gates in Figure 3 reset X1 X2 X3 and Y1 Y2 Y3 to 010. The comparator begins operating when START increases to 1, and Fig. 4(b) displays the timing diagram for this device. It is evident that the two propagating edges begin at the

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ISSN: XXXX-XXXX

same point [Fig. 4(b) shows that there is no initial phase difference between the two loops]. In this instance, the propagating edge of loop X is because Vip> Vin.

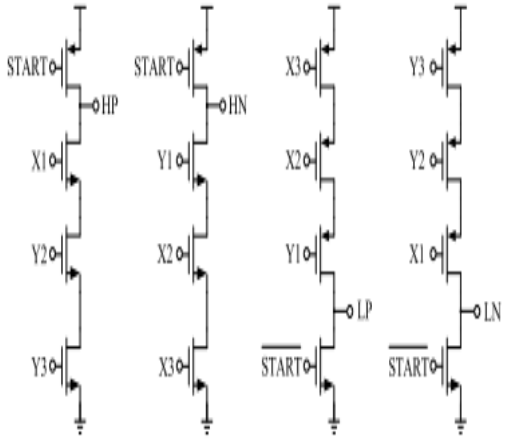

Fig. 5.Improved version of the circuit for measuring the distance.

Somewhat quicker than loop Y, which results in a progressive rise in the separation between the two propagating edges. X2, X3, and Y1 all rise at the same time at a significant distance [note the red-shaded areas in Fig. 4(b)], which lowers HN. HP doesn't alter and stays high throughout the interim. These comparative findings, which show HP = 1 and HN = 0, fit Vip> Vin rather well. Since the comparison continues until the edge distance grows to almost two inverter delays, the preset value d0 in this case is approximately two inverter delays. Let us examine Fig. 4(b) in more detail: The dropping edge of Y1 and X1 are the same at the beginning. Furthermore, only X2 and X3, excluding Y1, are high at the same time (the red shaded zone). Because loop Y is slower than loop X, the lowering edge of Y1 progressively moves into the red-shaded area over time. As a result, X2 X3 Y1 are all simultaneously high, ending the comparison. We determine that the preset value d0 is about two inverter delays because, at this point, the distance between the Y1 and X1 falling edges is approximately two inverter delays. A drawback of the circuit in Fig. 4(a) is that it can only detect the instant when X2, X3, and Y1 are all high at the same time; it cannot detect the same moment when X2, X3, and Y1 are all low at the same time. An enhanced version of the circuit is shown in Fig. 5 to get around this restriction. Figs. 4(a) and 5 are identical except for the two additional dynamic logics that are included for producing LP and LN. Both LP and LN are reset to low ("L" stands for low) during the reset phase (START = 0). Following the increase of START to 1, the circuit functions as shown in Fig. 4(a). The only distinction is that, as opposed to Fig. 4(a), which uses three nMOS transistors to bring down the voltage, it employs three pMOS transistors to pull up the output voltage, LP or LN. With this adjustment, the exact instant when X2, X3, and Y1 are all low at the same time is detected. In the meanwhile, Fig. 5's HP and HN branches function similarly to Fig. 4(a) in identifying the instant at which X2, X3, and Y1 are all concurrently high. The final circuit design is shown in Fig. 6, which should considerably enhance the performance of Fig. 5. Two changes are the only things that are different. To increase driving power and sharpen the edges, we first add inverters I1–I6. Secondly, in order to remove the coupling-related glitches in HP, HN, LP, and LN, we add

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additional transistors M17–M20. Glitches are evident in Fig. 5: we want HP, HN, LP, and LN to be the same after START increases but before the comparison result is created. But since HP, HN, LP, and LN are now floating in Fig. 5, they are really affected by the fluctuation in X1–X3 and Y1–Y3 due to the coupling of parasitic capacitances. To solve this problem, we include

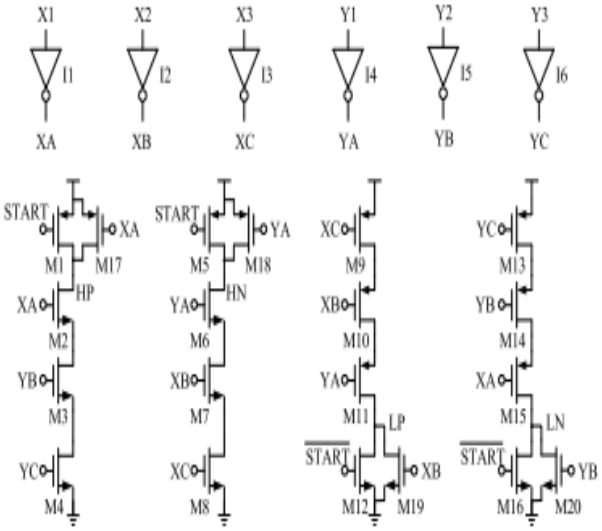

Fig. 6. Final version of the circuit for measuring the distance

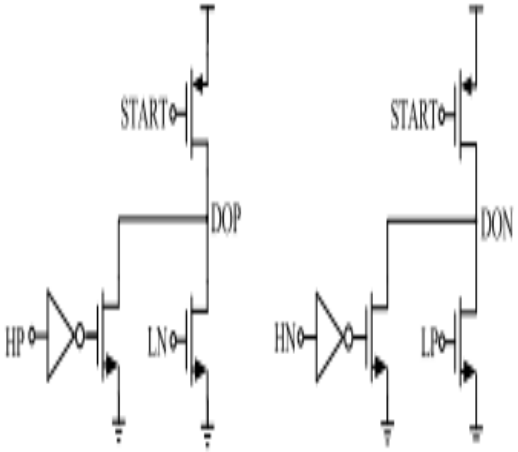

Fig. 7.Circuit to obtain the final comparison result.extra transistors M17–M20 into Fig. 6 to effectively reduce this disturbance.

The circuit for storing the comparison results is shown in Fig. 7. With one alteration, it is based on a traditional dynamic register circuit of [18]. We employ two nMOS transistors in each branch instead of just one as we need to aggregate the four results: HP, HN, LP, and LN. In this case, combining HP and LN yields the final DOP result, whereas combining HN and LP yields the final DON result.

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V. RESULTS

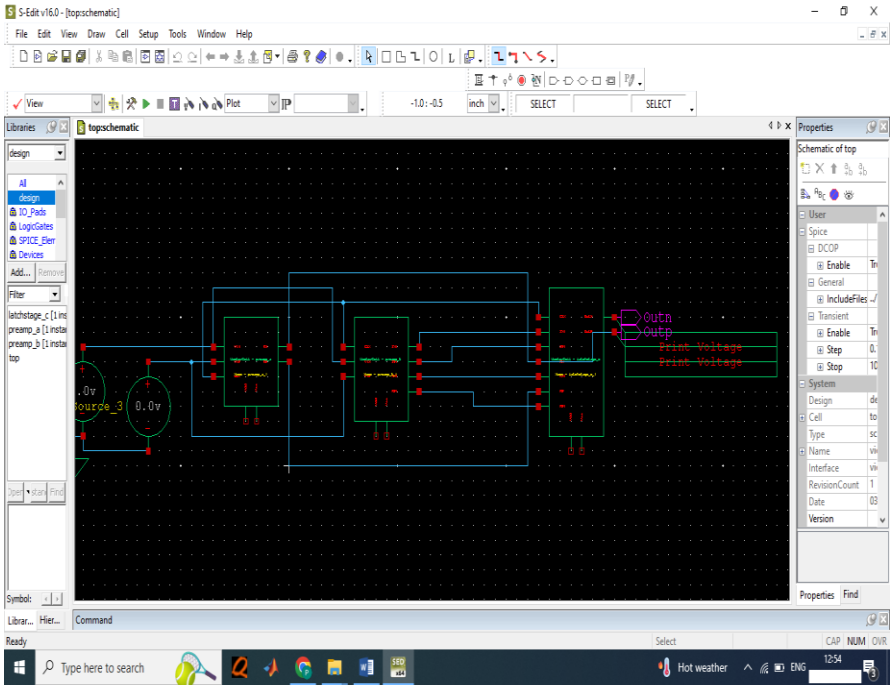

Fig:8 proposed block diagram

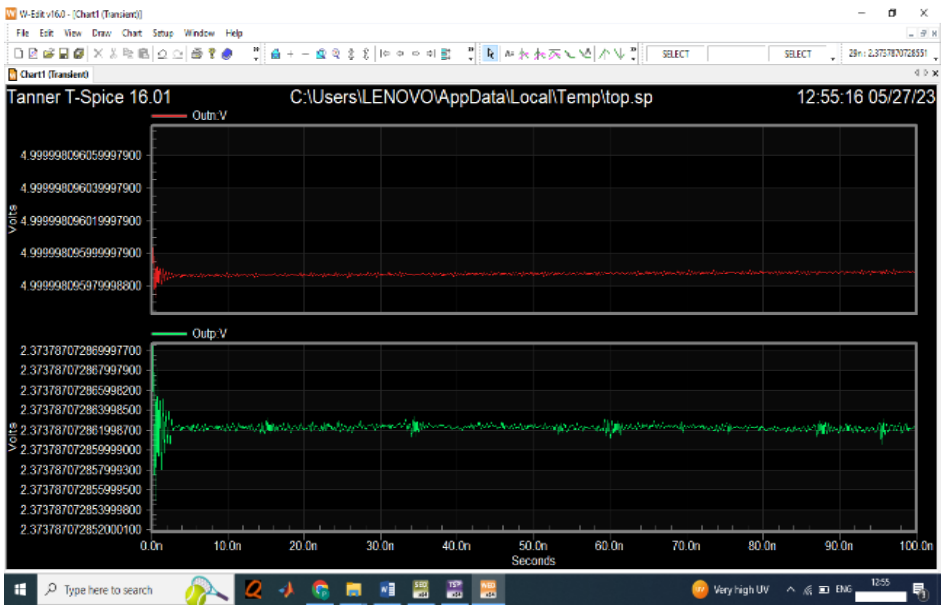

Fig9: proposed simulation result

Conclusion & Future Scope

A new voltage comparator for low power, high-resolution SAR ADCs is proposed in this paper. The suggested comparator speed is much higher and the power consumption is much lower than a previously published approach. The suggested structure is validated by the results of the simulation and measurements. In the future, one may lower the power consumption, hysteresis response, and input referred latch offset voltage. One issue might be the optimization of the circuits following layout and the offset voltage. Another problem is to find comparators that are particular to an application.

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